ABSTRACT OF THE DISCLOSURE

A logic in DRAM LSI is disclosed, which comprises a plurality of DRAM circuits, a control circuit that receives a test control signal to perform a test control in which the plurality of RAM circuits are tested while the access to the plurality of DRAM circuits is subsequently changed for each row, an input selector that is controlled by the control circuit and inputs a DRAM macro signal to the plurality of DRAM circuits at the time of a test, and an output selector that is controlled by the control circuit, and outputs output signals of the plurality of DRAM circuits sequentially to a macro output terminal at the time of the test. According to the DRAM integrated LSI, a test time required to test the plurality of DRAM circuits integrated in the LSI is shortened. Moreover, data that is read from the plurality of DRAM circuits is transferred in a high speed.